Sub A1

WHAT IS CLAIMED IS:

1. An information processing system comprising a memory unit and a memory controller, wherein said memory controller includes:

storing means for storing changeable memory control timing information;

monitoring means for monitoring an operating state of said memory unit;

a register for fetching the memory control timing information from said memory control timing information storing means; and

control means for controlling an access timing to said memory unit based on the memory control timing information in said register and for changing the information stored in said memory control timing information storing means based on information from said monitoring means.

2. A system according to claim 1, wherein:

said memory unit includes a mixture of a plurality of groups of memory elements different in operation, wherein said storing means for storing memory control timing information stores the memory control timing information corresponding to each of said groups of memory elements.

3. A system according to claim 1, wherein:

said memory unit comprises an environmental sensor for monitoring a temperature and a current, wherein said control means updates information stored

in said storing means so as to delay an operation timing to said memory unit in response to a notification indicating that a temperature rise around said memory unit or a current value from said environmental sensor exceeds a reference value.

4. A system according to claim 1, wherein:

said memory controller comprises a memory fault detector circuit, wherein said control means, in response to a detection by said detector circuit that a particular group of memory elements fails, updates stored information corresponding to said group of memory elements in said storing means so as to delay an operation timing to said memory unit.

5. A system according to claim 1, wherein:

said memory controller comprises a memory fault detector circuit, wherein said control means, in response to a detection by said detector circuit that a particular group of memory elements fails and that the fault is degraded performance in a particular operation, updates stored information corresponding to said group of memory elements in said storing means so as to delay an operation timing to said memory unit.

6. A memory controller for an information processing system, said memory controller adapted for connection with a processor and a memory unit, comprising:

storing means for storing changeable memory control timing information;

monitoring means for monitoring an operating state of said memory unit to issue information related with said operating state;

a register for fetching memory control timing information from said memory control timing information storing means; and

a control circuit for controlling an access timing of said memory unit based on the memory control timing information in said register and for changing the information stored in said memory control timing information storing means based on memory state information from said monitoring means.

7. A memory controller according to claim 6, wherein:

said memory unit includes an environmental sensor, wherein said change control circuit changes said timing information stored in said timing information storing means based on environmental data on said memory unit from said environmental sensor.

8. A memory controller according to claim 7, wherein:

said environmental data on said memory unit from said environmental sensor includes a change in temperature around said memory unit, and a current value of said memory unit.

9. A memory controller according to claim 6, wherein:

said memory unit includes a mixture of a

plurality of groups of memory elements different in operation; and

said timing information storage means stores memory control timing information corresponding to each said group of memory elements.

10. A memory controller according to claim 6, wherein:

said monitoring means includes a memory fault detector circuit for detecting a fault in a particular group of memory elements to output information indicative of the fault, wherein said change control circuit changes stored timing information corresponding to said group of memory elements in response to the output information from said memory fault detector circuit.

11. A memory controller according to claim 10, wherein:

the fault detected by said fault detector circuit is degraded performance in a particular operation of a group of memory elements.